TIMING PARAMETERS (ADSP-2111)

HOST INTERFACE PORT
Multiplexed Data & Address (HMD1 = 1)
Read/Write Strobe & Data Strobe (HMD0 = 1)

Parameter	13.0 MHz Min	13.0 MHz Max	16.67 MHz Min	16.67 MHz Max	20 MHz Min	20 MHz Max	*No Frequency Dependency*	Unit
Timing Requirement:								
t_{HALP} ALE Pulse Width	15		15		15			ns
t_{HASU} HAD15-0 Address Setup before ALE Low	5		5		5			ns
t_{HAH} HAD15-0 Address Hold after ALE Low	2		2		2			ns
t_{HALS} Start of Write or Read after ALE Low[1]	15		15		15			ns
t_{HSU} HRW Setup before Start of Write or Read[1]	8		8		8			ns
t_{HDSU} HAD15-0 Data Setup before End of Write[2]	5		5		5			ns
t_{HWDH} HAD15-0 Data Hold after End of Write[2]	3		3		3			ns
t_{HH} HRW Hold after End of Write or Read[2]	3		3		3			ns
t_{HRWP} Read or Write Pulse Width[3]	30		30		30			ns
Switching Characteristic:								
t_{HSHK} $\overline{HACK}$ Low after Start of Write or Read[1]	0	20	0	20	0	20		ns
t_{HKH} $\overline{HACK}$ Hold after End of Write or Read[2]	0	20	0	20	0	20		ns
t_{HDE} HAD15-0 Data Enabled after Start of Read[1]	0		0		0			ns
t_{HDD} HAD15-0 Data Valid after Start of Read[1]		23		23		23		ns
t_{HRDH} HAD15-0 Data Hold after End of Read[2]	0		0		0			ns
t_{HRDD} HAD15-0 Data Disabled after End of Read[2]		10		10		10		ns

NOTES
[1]Start of Write or Read = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.
[2]End of Write or Read = $\overline{HDS}$ High or $\overline{HSEL}$ High.
[3]Read or Write Pulse Width = $\overline{HDS}$ Low and $\overline{HSEL}$ Low.

Host Write Cycle

Host Read Cycle

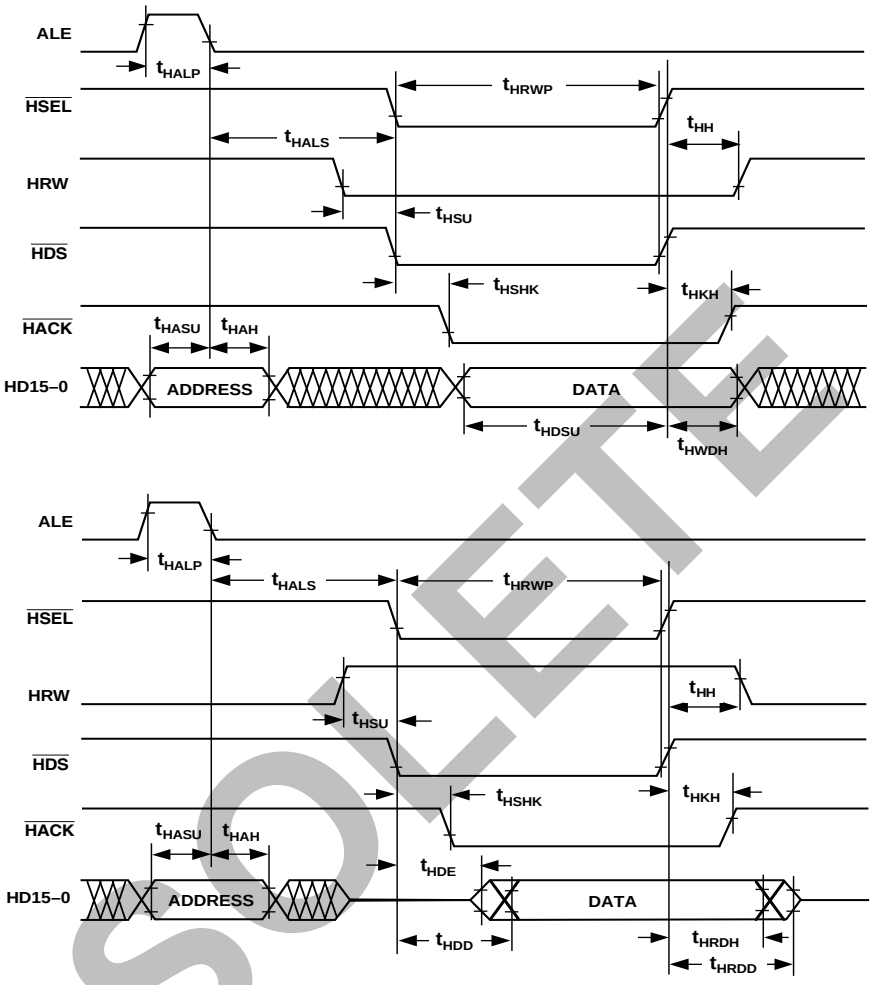


Figure 38. Host Interface Port (HMD1 = 1, HMD0 = 1)

TIMING PARAMETERS (ADSP-2103/2162/2164)

GENERAL NOTES

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

TIMING NOTES

Switching characteristics specify how the processor changes its signals. You have no control over this timing—circuitry external to the processor must be designed for compatibility with these signal characteristics. Switching characteristics tell you what the processor will do in a given circumstance. You can also use switching characteristics to ensure that any timing requirement of a device connected to the processor (such as memory) is satisfied.

Timing requirements apply to signals that are controlled by circuitry external to the processor, such as the data input for a read operation. Timing requirements guarantee that the processor operates correctly with other devices.

MEMORY REQUIREMENTS

The table below shows common memory device specifications and the corresponding ADSP-21xx timing parameters, for your convenience.

Memory Specification	ADSP-21xx Timing Parameter	Timing Parameter Definition
Address Setup to Write Start	t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low
Address Setup to Write End	t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Deasserted
Address Hold Time	t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold after $\overline{WR}$ Deasserted
Data Setup Time	t_{DW}	Data Setup before $\overline{WR}$ High
Data Hold Time	t_{DH}	Data Hold after $\overline{WR}$ High
$\overline{OE}$ to Data Valid	t_{RDD}	$\overline{RD}$ Low to Data Valid
Address Access Time	t_{AA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$ to Data Valid

TIMING PARAMETERS (ADSP-2103/2162/2164)

CLOCK SIGNALS & RESET

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{CK}	CLKIN Period	97.6	150			ns
t_{CKL}	CLKIN Width Low	20				ns
t_{CKH}	CLKIN Width High	20				ns
t_{RSP}	$\overline{\text{RESET}}$ Width Low	488		$5t_{CK}$[1]		ns
Switching Characteristic:						
t_{CPL}	CLKOUT Width Low	38.8		$0.5t_{CK} - 10$		ns
t_{CPH}	CLKOUT Width High	38.8		$0.5t_{CK} - 10$		ns
t_{CKOH}	CLKIN High to CLKOUT High	0	20			ns

NOTES
[1]Applies after powerup sequence is complete. Internal phase lock loop requires no more than 2000 CLKIN cycles assuming stable CLKIN (not including crystal oscillator startup time).

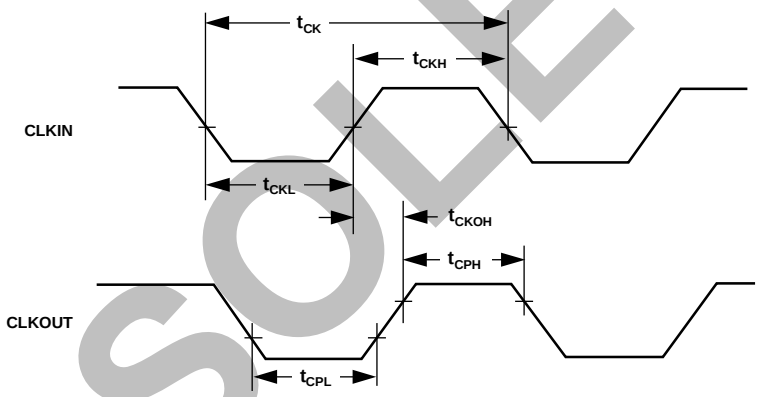


Figure 39. Clock Signals

TIMING PARAMETERS (ADSP-2103/2162/2164)

INTERRUPTS & FLAGS

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{IFS}	$\overline{IRQx}$[1] or FI Setup before CLKOUT Low[2, 3]	44.4		$0.25t_{CK}$ + 20		ns
t_{IFH}	$\overline{IRQx}$[1] or FI Hold after CLKOUT High[2, 3]	24.4		$0.25t_{CK}$		ns
Switching Characteristic:						
t_{FOH}	FO Hold after CLKOUT High	0				ns
t_{FOD}	FO Delay from CLKOUT High		15			ns

NOTES
[1]$\overline{IRQx}$=$\overline{IRQ0}$, $\overline{IRQ1}$, and $\overline{IRQ2}$.
[2]If $\overline{IRQx}$ and FI inputs meet t_{IFS} and t_{IFH} setup/hold requirements, they will be recognized during the current clock cycle; otherwise they will be recognized during the following cycle. (Refer to the "Interrupt Controller" section in Chapter 3, Program Control, of the *ADSP-2100 Family User's Manual* for further information on interrupt servicing.)
[3]Edge-sensitive interrupts require pulse widths greater than 10 ns. Level-sensitive interrupts must be held low until serviced.

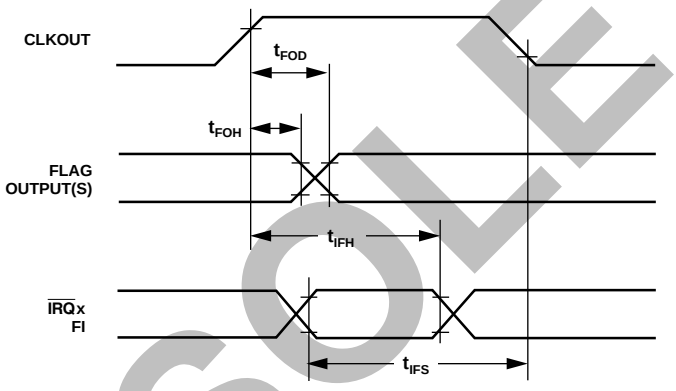


Figure 40. Interrupts & Flags

TIMING PARAMETERS (ADSP-2103/2162/2164)

BUS REQUEST/GRANT

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{BH}	$\overline{BR}$ Hold after CLKOUT High[1]	29.4		$0.25t_{CK}$ + 5		ns
t_{BS}	$\overline{BR}$ Setup before CLKOUT Low[1]	44.4		$0.25t_{CK}$ + 20		ns
Switching Characteristic:						
t_{SD}	CLKOUT High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable		44.4		$0.25t_{CK}$ + 20	ns
t_{SDB}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Disable to $\overline{BG}$ Low	0				ns
t_{SE}	$\overline{BG}$ High to $\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable	0				ns
t_{SEC}	$\overline{DMS}$, $\overline{PMS}$, $\overline{BMS}$, $\overline{RD}$, $\overline{WR}$ Enable to CLKOUT High	14.4		$0.25t_{CK}$ – 10		ns

NOTES

[1]If $\overline{BR}$ meets the t_{BS} and t_{BH} setup/hold requirements, it will be recognized in the current processor cycle; otherwise it is recognized in the following cycle. $\overline{BR}$ requires a pulse width greater than 10 ns.

Section 10.2.4, "Bus Request/Grant," of the *ADSP-2100 Family User's Manual (1st Edition, ©1993)* states that "When $\overline{BR}$ is recognized, the processor responds immediately by asserting $\overline{BG}$ during the same cycle." This is incorrect for the current versions of all ADSP-21xx processors: $\overline{BG}$ is asserted in the cycle after $\overline{BR}$ is recognized. No external synchronization circuit is needed when $\overline{BR}$ is generated as an asynchronous signal.

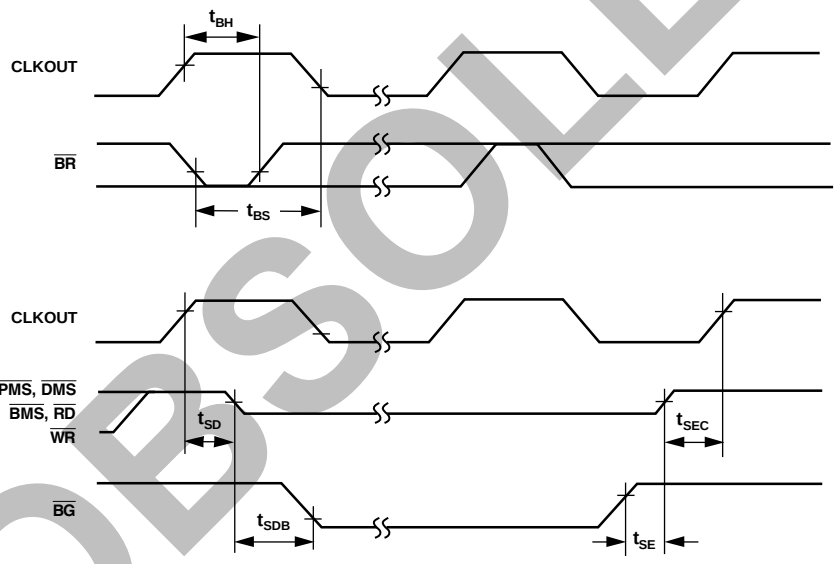


Figure 41. Bus Request/Grant

TIMING PARAMETERS (ADSP-2103/2162/2164)

MEMORY READ

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{RDD}	$\overline{RD}$ Low to Data Valid		33.8		$0.5t_{CK} - 15 + w$	ns
t_{AA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ to Data Valid		49.2		$0.75t_{CK} - 24 + w$	ns
t_{RDH}	Data Hold from $\overline{RD}$ High	0				ns
Switching Characteristic:						
t_{RP}	$\overline{RD}$ Pulse Width	43.8		$0.5t_{CK} - 5 + w$		ns
t_{CRD}	CLKOUT High to $\overline{RD}$ Low	19.4	34.4	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{ASR}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Setup before $\overline{RD}$ Low	12.4		$0.25t_{CK} - 12$		ns
t_{RDA}	A0–A13, $\overline{PMS}$, $\overline{DMS}$, $\overline{BMS}$ Hold after $\overline{RD}$ Deasserted	14.4		$0.25t_{CK} - 10$		ns
t_{RWR}	$\overline{RD}$ High to $\overline{RD}$ or $\overline{WR}$ Low	38.8		$0.5t_{CK} - 10$		ns

w = wait states × t_{CK}.

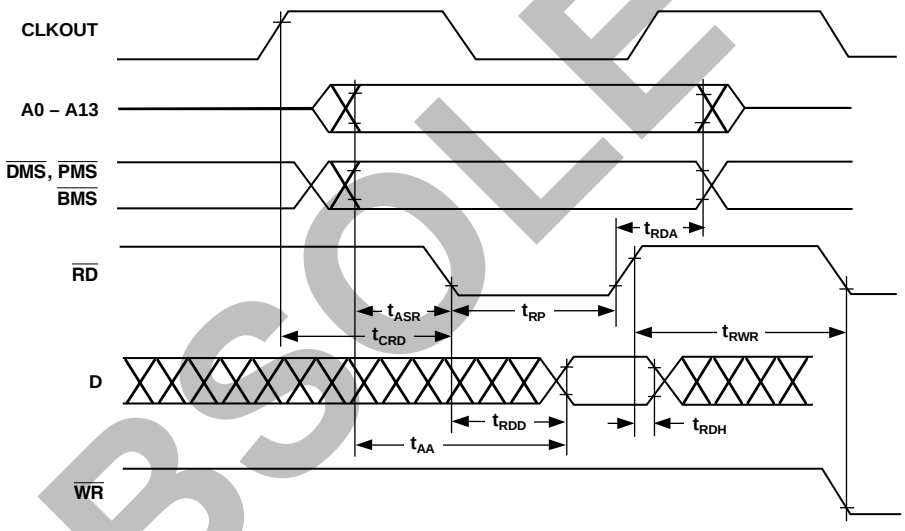


Figure 42. Memory Read

TIMING PARAMETERS (ADSP-2103/2162/2164)

MEMORY WRITE

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Switching Characteristic:						
t_{DW}	Data Setup before $\overline{WR}$ High	38.8		$0.5t_{CK} - 10 + w$		ns
t_{DH}	Data Hold after $\overline{WR}$ High	14.4		$0.25t_{CK} - 10$		ns
t_{WP}	$\overline{WR}$ Pulse Width	43.8		$0.5t_{CK} - 5 + w$		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	0				
t_{ASW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Setup before $\overline{WR}$ Low	12.4		$0.25t_{CK} - 12$		ns
t_{DDR}	Data Disable before $\overline{WR}$ or $\overline{RD}$ Low	14.4		$0.25t_{CK} - 10$		ns
t_{CWR}	CLKOUT High to $\overline{WR}$ Low	19.4	34.4	$0.25t_{CK} - 5$	$0.25t_{CK} + 10$	ns
t_{AW}	A0–A13, $\overline{DMS}$, $\overline{PMS}$, Setup before $\overline{WR}$ Deasserted	58.2		$0.75t_{CK} - 15 + w$		ns
t_{WRA}	A0–A13, $\overline{DMS}$, $\overline{PMS}$ Hold After $\overline{WR}$ Deasserted	14.4		$0.25t_{CK} - 10$		ns
t_{WWR}	$\overline{WR}$ High to $\overline{RD}$ or $\overline{WR}$ Low	38.8		$0.5t_{CK} - 10$		ns

w = wait states × t_{CK}.

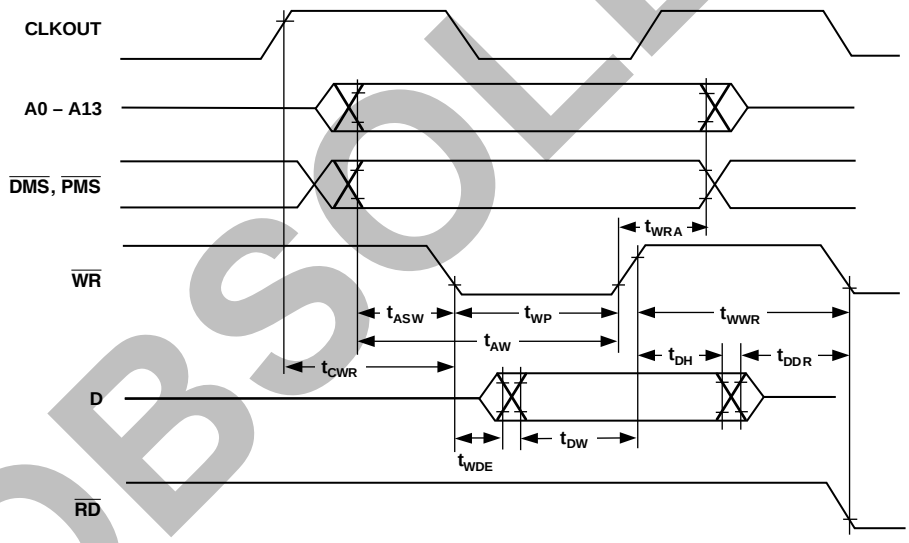


Figure 43. Memory Write

TIMING PARAMETERS (ADSP-2103/2162/2164)

SERIAL PORTS

Parameter		10.24 MHz Min	10.24 MHz Max	Frequency Dependency Min	Frequency Dependency Max	Unit
Timing Requirement:						
t_{SCK}	SCLK Period	97.6		t_{CK}		ns
t_{SCS}	DR/TFS/RFS Setup before SCLK Low	8				ns
t_{SCH}	DR/TFS/RFS Hold after SCLK Low	10				ns
t_{SCP}	$SCLK_{in}$ Width	28				ns
Switching Characteristic:						
t_{CC}	CLKOUT High to $SCLK_{out}$	24.4	39.4	$0.25t_{CK}$	$0.25t_{CK}$ + 15	ns
t_{SCDE}	SCLK High to DT Enable	0				ns
t_{SCDV}	SCLK High to DT Valid		28			ns
t_{RH}	TFS/RFS_{out} Hold after SCLK High	0				ns
t_{RD}	TFS/RFS_{out} Delay from SCLK High		28			ns
t_{SCDH}	DT Hold after SCLK High	0				ns
t_{TDE}	TFS (alt) to DT Enable	0				ns
t_{TDV}	TFS (alt) to DT Valid		18			ns
t_{SCDD}	SCLK High to DT Disable		30			ns
t_{RDV}	RFS (Multichannel, Frame Delay Zero) to DT Valid		20			ns

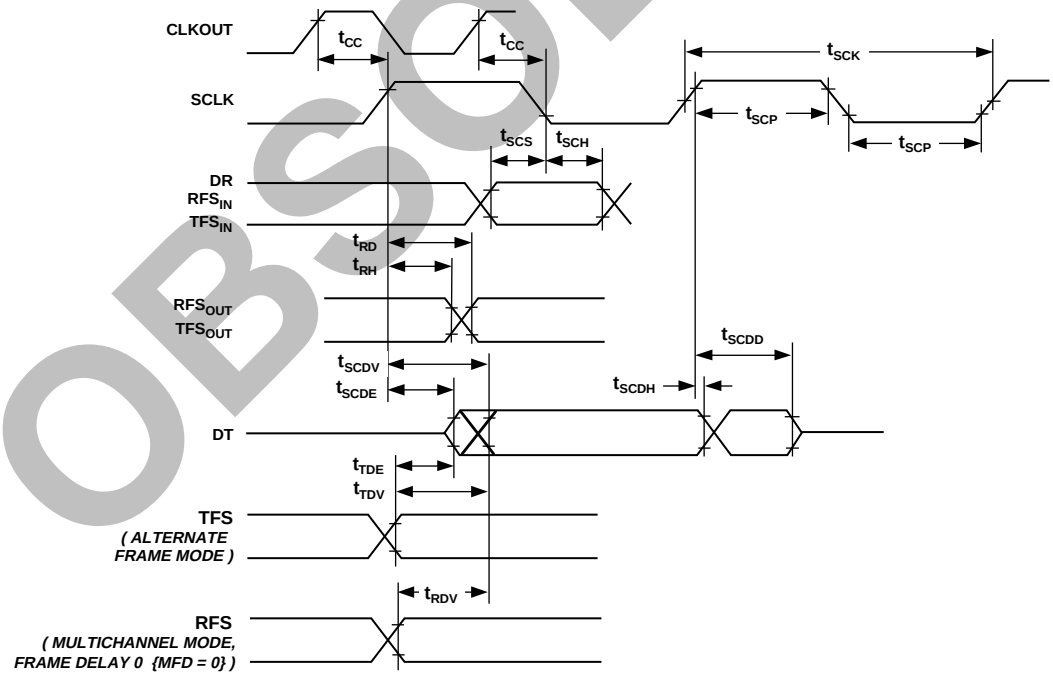
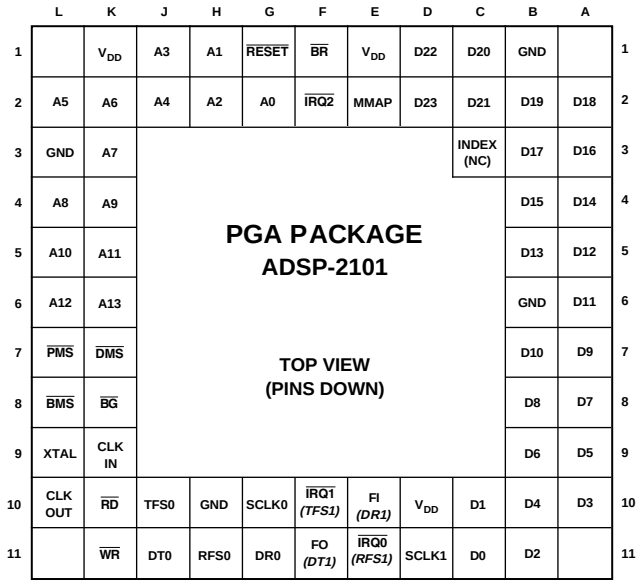
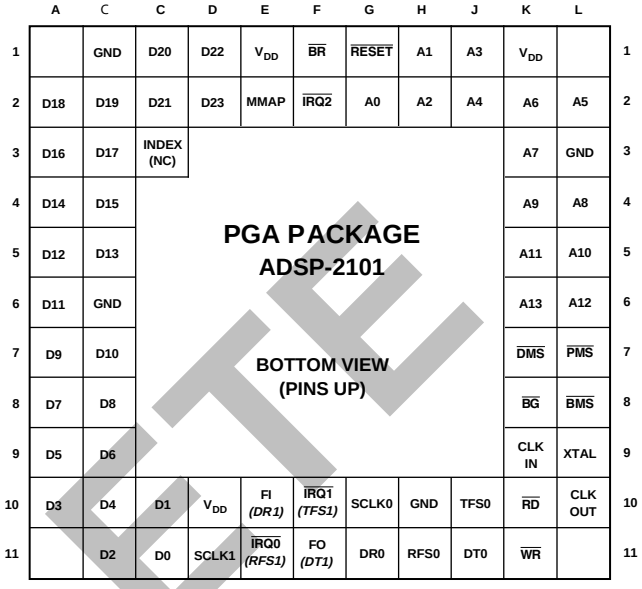


Figure 44. Serial Ports

PIN CONFIGURATIONS

68-Pin PGA





NC = NO CONNECT

PGA Number	Pin Name
K11	$\overline{WR}$
K10	$\overline{RD}$
J11	DT0
J10	TFS0
H11	RFS0
H10	GND
G11	DR0
G10	SCLK0
F11	FO *(DT1)*
F10	$\overline{IRQ1}$ *(TFS1)*
E11	$\overline{IRQ0}$ *(RFS1)*
E10	FI *(DR1)*
D11	SCLK1
D10	V_{DD}
C11	D0
C10	D1
B11	D2

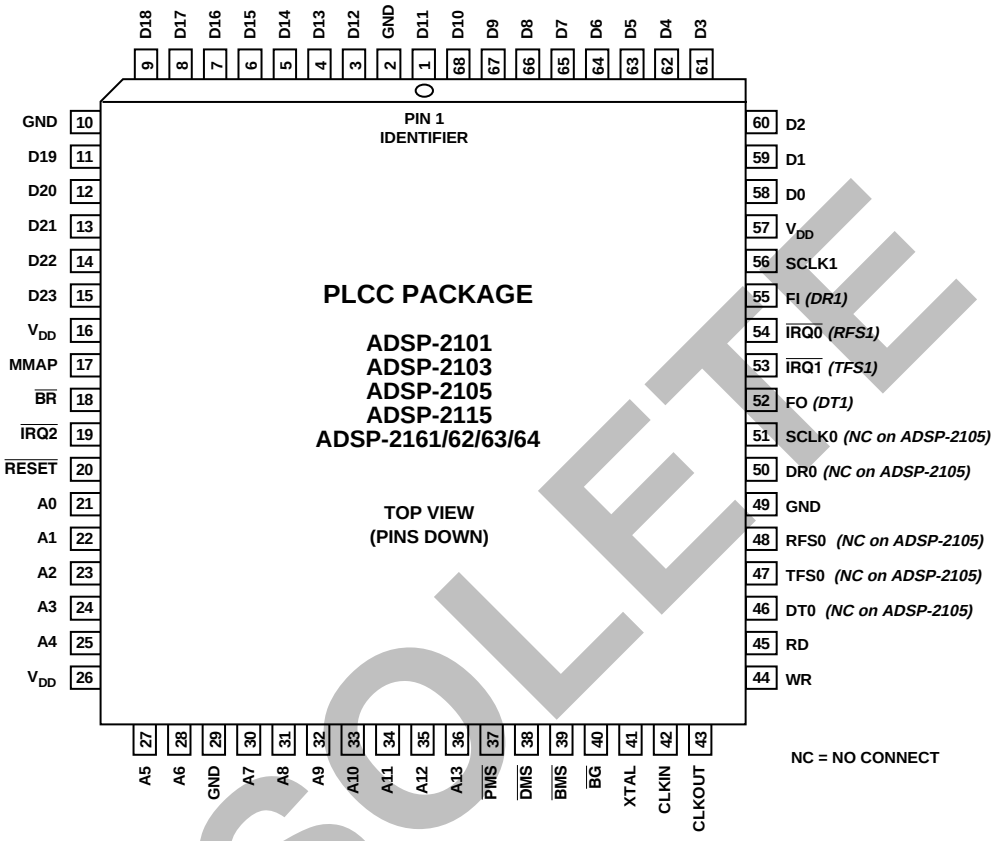
PGA Number	Pin Name
A10	D3
B10	D4
A9	D5
B9	D6
A8	D7
B8	D8
A7	D9
B7	D10
A6	D11
B6	GND
A5	D12
B5	D13
A4	D14
B4	D15
A3	D16
B3	D17
A2	D18

PGA Number	Pin Name
B1	GND
B2	D19
C1	D20
C2	D21
D1	D22
D2	D23
E1	V_{DD}
E2	MMAP
F1	$\overline{BR}$
F2	$\overline{IRQ2}$
G1	$\overline{RESET}$
G2	A0
H1	A1
H2	A2
J1	A3
J2	A4
K1	V_{DD}

PGA Number	Pin Name
L2	A5
K2	A6
L3	GND
K3	A7
L4	A8
K4	A9
L5	A10
K5	A11
L6	A12
K6	A13
L7	$\overline{PMS}$
K7	$\overline{DMS}$
L8	$\overline{BMS}$
K8	$\overline{BG}$
L9	XTAL
K9	CLKIN
L10	CLKOUT
C3	Index (NC)

PIN CONFIGURATIONS

68-Lead PLCC



PLCC Number	Pin Name
1	D11
2	GND
3	D12
4	D13
5	D14
6	D15
7	D16
8	D17
9	D18
10	GND
11	D19
12	D20
13	D21
14	D22
15	D23
16	V_{DD}
17	MMAP

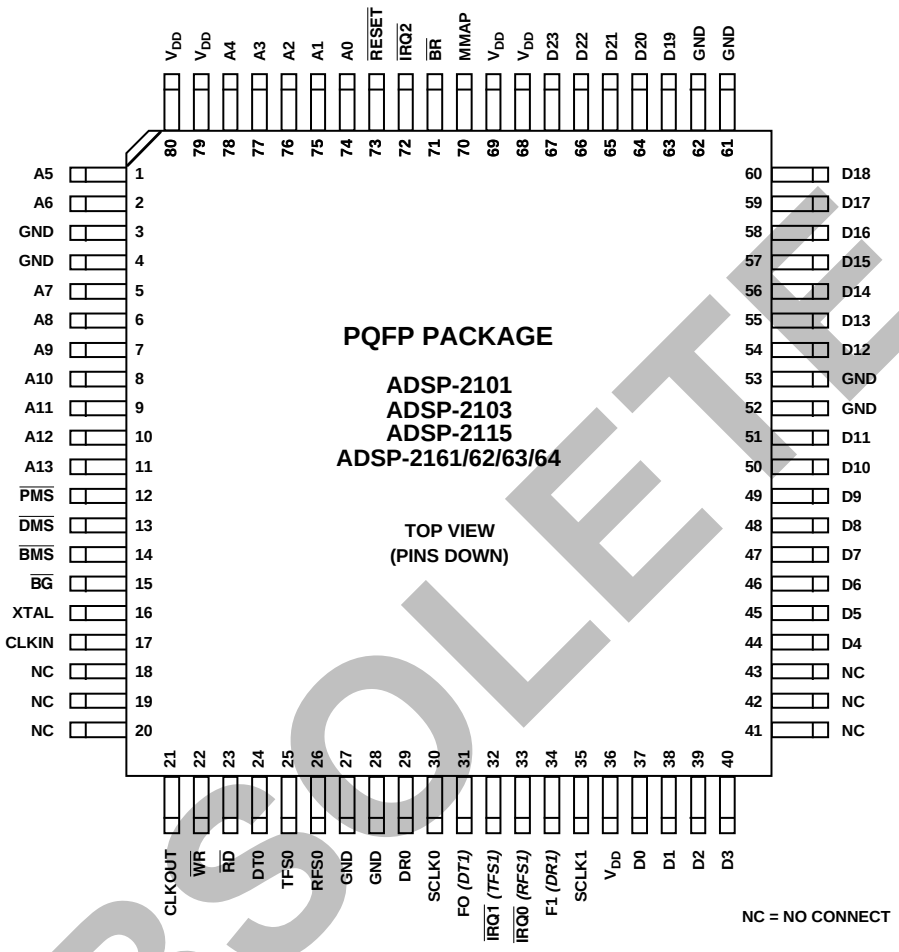
PLCC Number	Pin Name
18	$\overline{BR}$
19	$\overline{IRQ2}$
20	$\overline{RESET}$
21	A0
22	A1
23	A2
24	A3
25	A4
26	V_{DD}
27	A5
28	A6
29	GND
30	A7
31	A8
32	A9
33	A10
34	A11

PLCC Number	Pin Name
35	A12
36	A13
37	$\overline{PMS}$
38	$\overline{DMS}$
39	$\overline{BMS}$
40	$\overline{BG}$
41	XTAL
42	CLKIN
43	CLKOUT
44	$\overline{WR}$
45	$\overline{RD}$
46	DT0 *(NC on ADSP-2105)*
47	TFS0 *(NC on ADSP-2105)*
48	RFS0 *(NC on ADSP-2105)*
49	GND
50	DR0 *(NC on ADSP-2105)*
51	SCLK0 *(NC on ADSP-2105)*

PLCC Number	Pin Name
52	FO *(DT1)*
53	$\overline{IRQ1}$ *(TFS1)*
54	$\overline{IRQ0}$ *(RFS1)*
55	FI *(DR1)*
56	SCLK1
57	V_{DD}
58	D0
59	D1
60	D2
61	D3
62	D4
63	D5
64	D6
65	D7
66	D8
67	D9
68	D10

PIN CONFIGURATIONS

80-Lead PQFP
80-Lead TQFP



PQFP/ TQFP Number	Pin Name
1	A5
2	A6
3	GND
4	GND
5	A7
6	A8
7	A9
8	A10
9	A11
10	A12
11	A13
12	$\overline{\text{PMS}}$
13	$\overline{\text{DMS}}$
14	$\overline{\text{BMS}}$
15	$\overline{\text{BG}}$
16	XTAL
17	CLKIN
18	NC
19	NC
20	NC

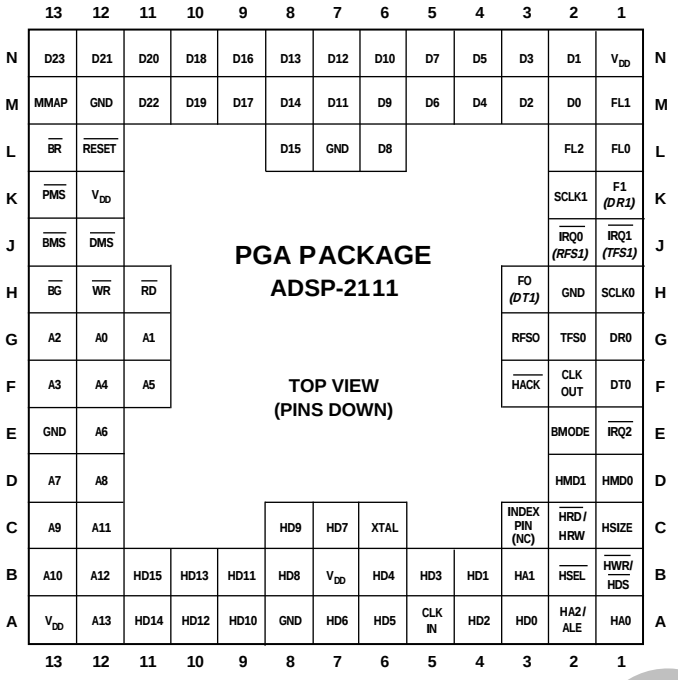
PQFP/ TQFP Number	Pin Name
21	CLKOUT
22	$\overline{\text{WR}}$
23	$\overline{\text{RD}}$
24	DT0
25	TFS0
26	RFS0
27	GND
28	GND
29	DR0
30	SCLK0
31	FO *(DT1)*
32	$\overline{\text{IRQ1}}$ *(TFS1)*
33	$\overline{\text{IRQ0}}$ *(RFS1)*
34	FI *(DR1)*
35	SCLK1
36	V_{DD}
37	D0
38	D1
39	D2
40	D3

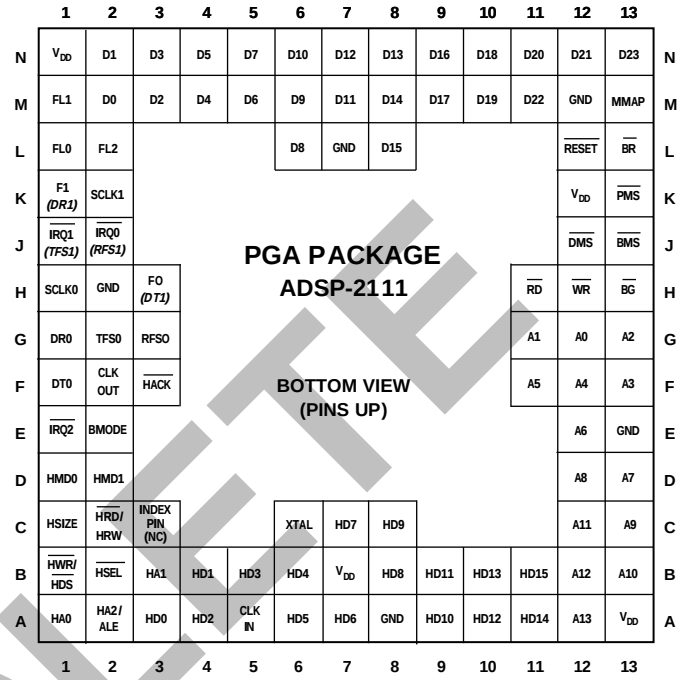
PQFP/ TQFP Number	Pin Name
41	NC
42	NC
43	NC
44	D4
45	D5
46	D6
47	D7
48	D8
49	D9
50	D10
51	D11
52	GND
53	GND
54	D12
55	D13
56	D14
57	D15
58	D16
59	D17
60	D18

PQFP/ TQFP Number	Pin Name
61	GND
62	GND
63	D19
64	D20
65	D21
66	D22
67	D23
68	V_{DD}
69	V_{DD}
70	MMAP
71	$\overline{\text{BR}}$
72	$\overline{\text{IRQ2}}$
73	$\overline{\text{RESET}}$
74	A0
75	A1
76	A2
77	A3
78	A4
79	V_{DD}
80	V_{DD}

PIN CONFIGURATIONS

100-Pin PGA





NC = NO CONNECT

PGA Number	Pin Name
N13	D23
N12	D21
M13	MMAP
M12	GND
L13	$\overline{BR}$
L12	$\overline{RESET}$
K13	$\overline{PMS}$
K12	V_{DD}
J13	$\overline{BMS}$
J12	$\overline{DMS}$
H13	$\overline{BG}$
H12	$\overline{WR}$
H11	$\overline{RD}$
G13	A2
G12	A0
G11	A1
F13	A3
F12	A4
F11	A5
E13	GND
E12	A6
D13	A7
D12	A8
C13	A9
C12	A11

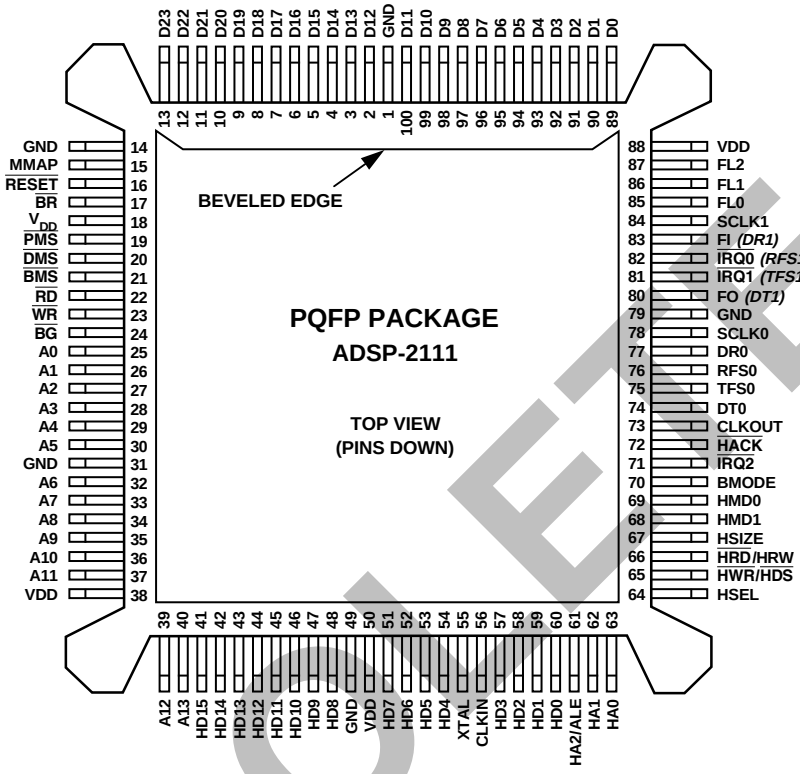
PGA Number	Pin Name
B13	A10
A13	V_{DD}
A12	A13
B12	A12
A11	HD14
B11	HD15
A10	HD12
B10	HD13
A9	HD10
B9	HD11
A8	GND
B8	HD8
C8	HD9
A7	HD6
B7	V_{DD}
C7	HD7
A6	HD5
B6	HD4
C6	XTAL
A5	CLKIN
B5	HD3
A4	HD2
B4	HD1
A3	HD0
B3	HA1

PGA Number	Pin Name
C3	Index (NC)
A2	HA2/ALE
A1	HA0
B1	$\overline{HWR}/\overline{HDS}$
B2	$\overline{HSEL}$
C1	HSIZE
C2	$\overline{HRD}$/HRW
D1	HMD0
D2	HMD1
E1	$\overline{IRQ2}$
E2	BMODE
F1	DT0
F2	CLKOUT
F3	$\overline{HACK}$
G1	DR0
G2	TFS0
G3	RFS0
H1	SCLK0
H2	GND
H3	FO *(DT1)*
J1	$\overline{IRQ1}$ *(TFS1)*
J2	$\overline{IRQ0}$ *(RFS1)*
K1	FI *(DR1)*
K2	SCLK1
L1	FL0

PGA Number	Pin Name
L2	FL2
M1	FL1
N1	V_{DD}
N2	D1
M2	D0
N3	D3
M3	D2
N4	D5
M4	D4
N5	D7
M5	D6
N6	D10
M6	D9
L6	D8
N7	D12
M7	D11
L7	GND
N8	D13
M8	D14
L8	D15
N9	D16
M9	D17
N10	D18
M10	D19
N11	D20
M11	D22

PIN CONFIGURATIONS

100-Lead Bumpered PQFP



NOTE: PIN 1 IS LOCATED AT THE CENTER OF THE BEVELED-EDGE SIDE OF THE PACKAGE.

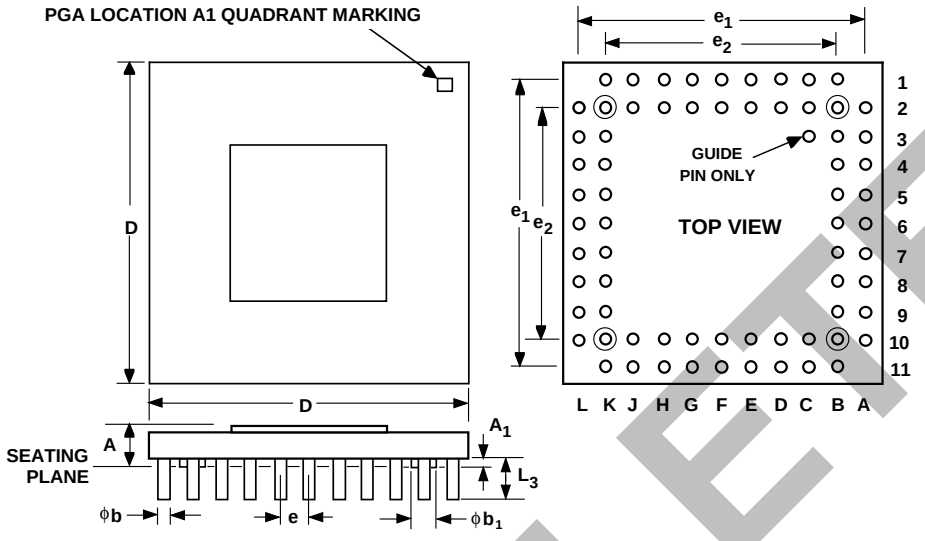
PQFP Number	Pin Name
1	GND
2	D12
3	D13
4	D14
5	D15
6	D16
7	D17
8	D18
9	D19
10	D20
11	D21
12	D22
13	D23
14	GND
15	MMAP
16	$\overline{\text{RESET}}$
17	$\overline{\text{BR}}$
18	V_{DD}
19	$\overline{\text{PMS}}$
20	$\overline{\text{DMS}}$
21	$\overline{\text{BMS}}$
22	$\overline{\text{RD}}$
23	$\overline{\text{WR}}$
24	$\overline{\text{BG}}$
25	A0

PQFP Number	Pin Name
26	A1
27	A2
28	A3
29	A4
30	A5
31	GND
32	A6
33	A7
34	A8
35	A9
36	A10
37	A11
38	V_{DD}
39	A12
40	A13
41	HD15
42	HD14
43	HD13
44	HD12
45	HD11
46	HD10
47	HD9
48	HD8
49	GND
50	V_{DD}

PQFP Number	Pin Name
51	HD7
52	HD6
53	HD5
54	HD4
55	XTAL
56	CLKIN
57	HD3
58	HD2
59	HD1
60	HD0
61	HA2/ALE
62	HA1
63	HA0
64	$\overline{\text{HSEL}}$
65	$\overline{\text{HWR}}$/$\overline{\text{HDS}}$
66	$\overline{\text{HRD}}$/HRW
67	HSIZE
68	HMD1
69	HMD0
70	BMODE
71	$\overline{\text{IRQ2}}$
72	$\overline{\text{HACK}}$
73	CLKOUT
74	DT0
75	TFS0

PQFP Number	Pin Name
76	RFS0
77	DR0
78	SCLK0
79	GND
80	$\overline{\text{FO}}$ *(DT1)*
81	$\overline{\text{IRQ1}}$ *(TFS1)*
82	$\overline{\text{IRQ0}}$ *(RFS1)*
83	FI *(DR1)*
84	SCLK1
85	FL0
86	FL1
87	FL2
88	V_{DD}
89	D0
90	D1
91	D2
92	D3
93	D4
94	D5
95	D6
96	D7
97	D8
98	D9
99	D10
100	D11

OUTLINE DIMENSIONS
ADSP-2101
68-Pin Grid Array (PGA)

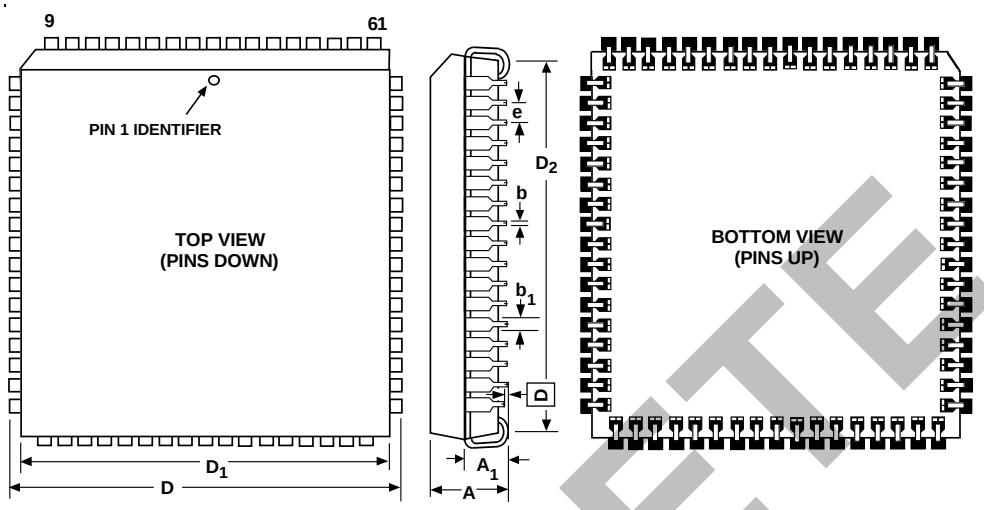


SYMBOL	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.123		0.164	3.12		4.17
A_1		0.50			1.27	
φb	0.016	0.018	0.020		0.46	
$φb_1$		0.050			1.27	
D	1.086		1.110	27.58		28.19
e_1	0.988		1.012	25.10		25.70
e_2	0.788		0.812	20.02		20.62
e		0.100			2.54	
L_3		0.180			4.57	

OUTLINE DIMENSIONS

ADSP-21xx

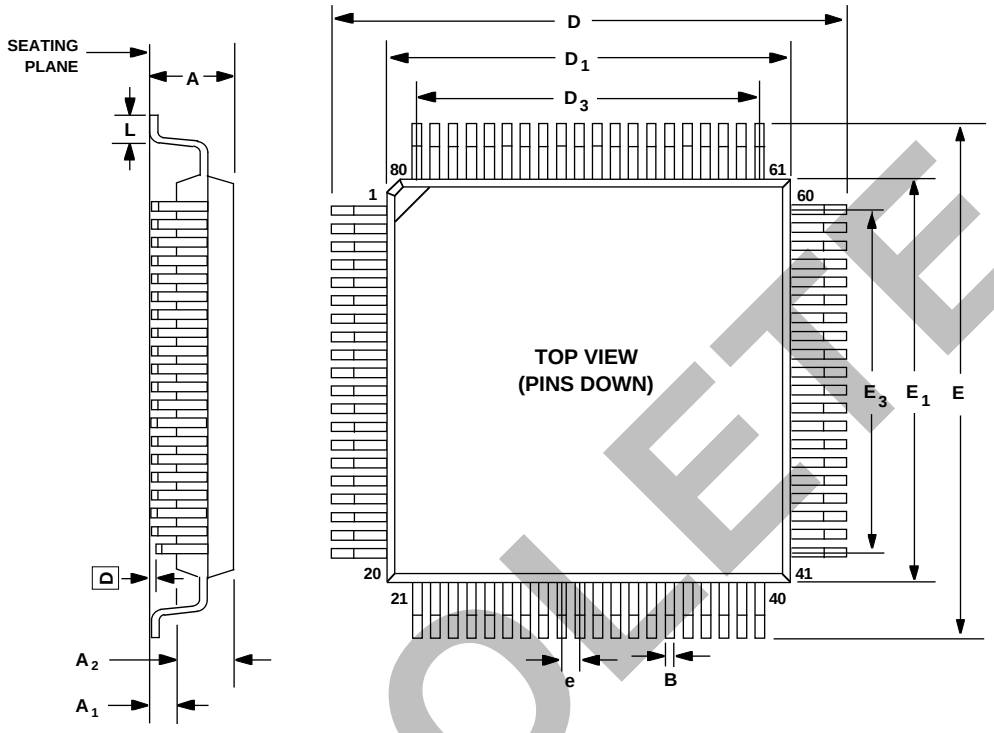
68-Lead Plastic Leaded Chip Carrier (PLCC)



SYMBOL	INCHES			MILLIMETERS		
	MIN	TYP	MAX	MIN	TYP	MAX
A	0.169	0.172	0.175	4.29	4.37	4.45
A_1		0.104			2.64	
b	0.017	0.018	0.019	0.43	0.46	0.48
b_1	0.027	0.028	0.029	0.69	0.71	0.74
D	0.985	0.990	0.995	25.02	25.15	25.27
D_1	0.950	0.952	0.954	24.13	24.18	24.23
D_2	0.895	0.910	0.925	22.73	23.11	23.50
e		0.050			1.27	
α			0.004			0.10

OUTLINE DIMENSIONS

ADSP-21xx
80-Lead Metric Plastic Quad Flatpack (PQFP)
80-Lead Metric Thin Quad Flatpack (TQFP)



PQFP

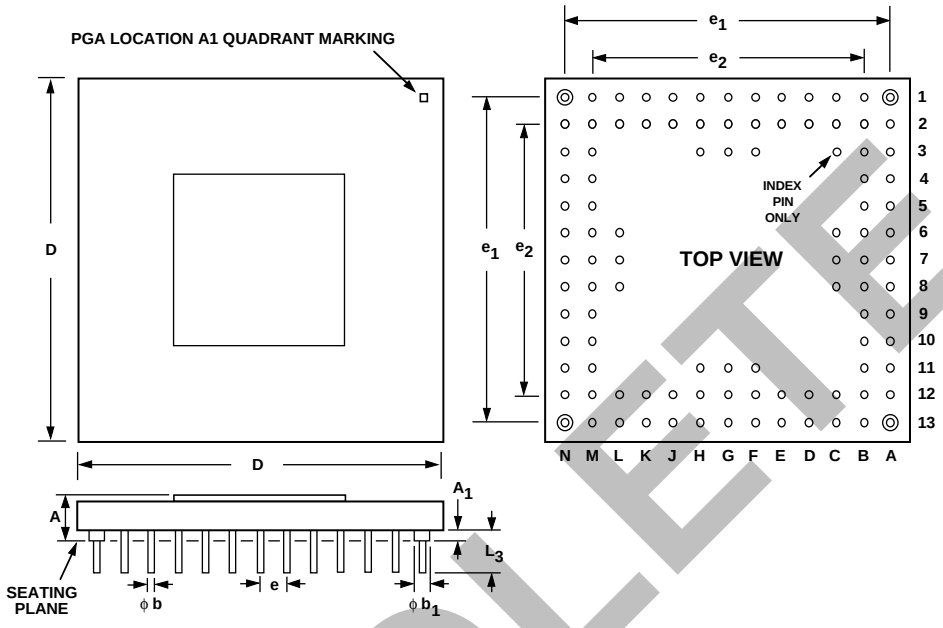
SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP	MAX	MIN	TYP	MAX
A			2.45			0.096
A_1	0.25			0.010		
A_2	1.90	2.00	2.10	0.075	0.079	0.083
D, E	16.95	17.20	17.45	0.667	0.678	0.690
D_1, E_1	13.90	14.00	14.10	0.547	0.551	0.555
D_3, E_3		12.35	12.43		0.486	0.490
L	0.65	0.80	0.95	0.026	0.031	0.037
e	0.57	0.65	0.73	0.023	0.026	0.029
B	0.22	0.30	0.38	0.009	0.012	0.015
c			0.10			0.004

TQFP

MILLIMETERS			INCHES		
MIN	TYP	MAX	MIN	TYP	MAX
		1.60			0.063
0.05		0.15	0.002		0.006
1.35	1.40	1.45	0.053	0.055	0.057
15.75	16.00	16.25	0.620	0.630	0.640
13.95	14.00	14.05	0.549	0.551	0.553
	12.35	12.43		0.486	0.490
0.50	0.60	0.75	0.020	0.024	0.030
0.57	0.65	0.73	0.022	0.026	0.029
0.25	0.30	0.35	0.010	0.012	0.014
		0.10			0.004

OUTLINE DIMENSIONS

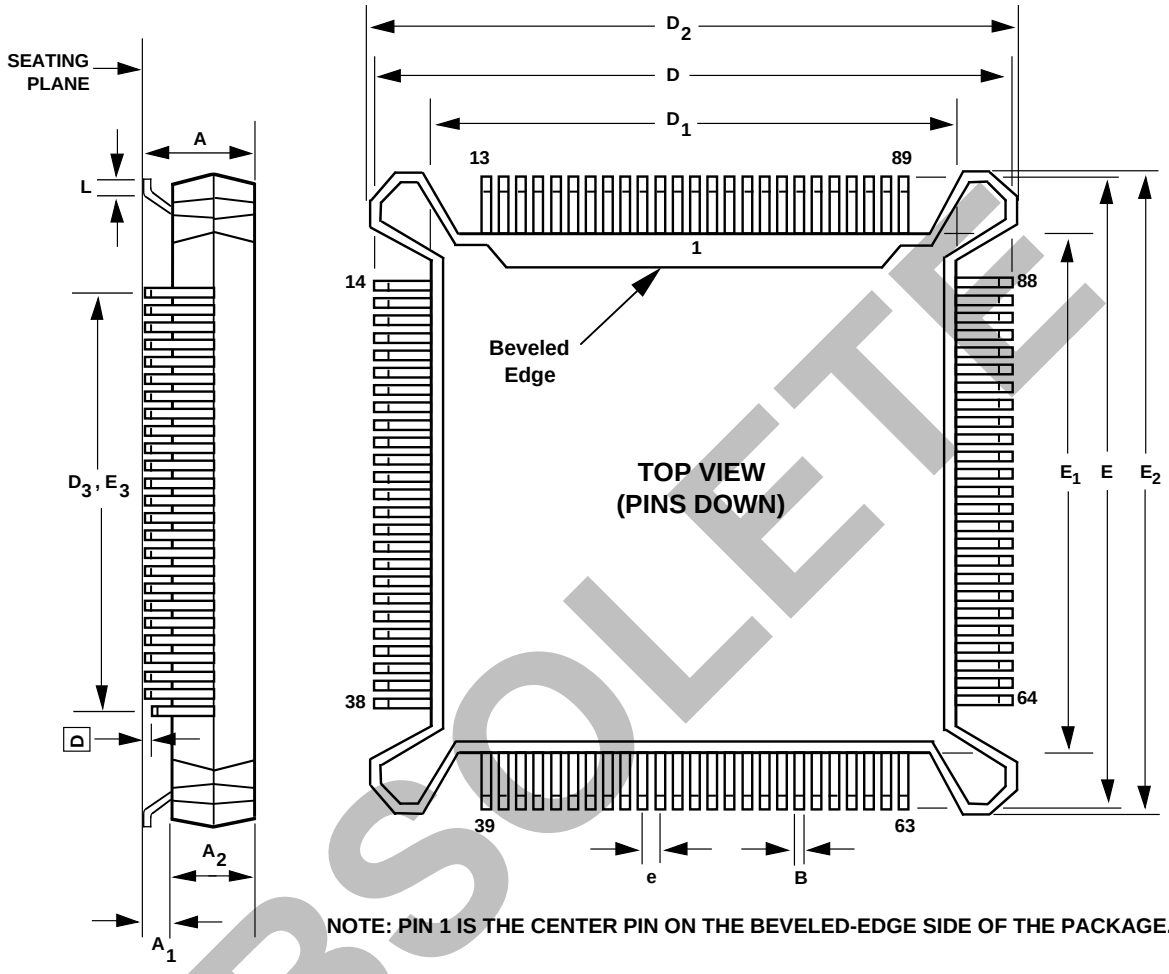
ADSP-2111
100-Pin Grid Array (PGA)



	INCHES			MILLIMETERS		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A	0.123		0.169	3.12		4.29
A_1		0.050			1.27	
ϕb	0.016	0.018	0.020	0.41	0.46	0.51
ϕb_1		0.050			1.27	
D	1.308	1.32	1.342	33.22	33.53	34.09
e_1	1.188	1.20	1.212	30.18	30.48	30.78
e_2	0.988	1.00	1.012	25.10	25.4	25.70
e		0.100			2.54	
L_3		0.180			4.57	

OUTLINE DIMENSIONS

ADSP-2111
100-Lead Bumpered Plastic Quad Flatpack (PQFP)



NOTE: PIN 1 IS THE CENTER PIN ON THE BEVELED-EDGE SIDE OF THE PACKAGE.

	INCHES			MILLIMETERS		
SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX
A			0.180			4.572
A_1	0.020	0.030	0.040	0.508	0.762	1.016
A_2	0.130	0.140	0.150	3.302	3.556	3.810
D, E	0.875	0.880	0.885	22.225	22.352	22.479
D_1, E_1	0.747	0.750	0.753	18.974	19.050	19.126
D_2, E_2	0.897	0.900	0.903	22.784	22.860	22.936
D_3, E_3		0.600	0.603		15.240	15.316
L	0.036		0.046	0.914		1.168
e	0.022	0.025	0.028	0.559	0.635	0.711
B	0.008		0.012	0.203		0.305
D			0.004			0.102

ORDERING GUIDE

Part Number[1]	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2101KG-66	0°C to +70°C	16.67 MHz	68-Pin PGA	G-68A
ADSP-2101BG-66	–40°C to +85°C	16.67 MHz	68-Pin PGA	G-68A
ADSP-2101KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2101BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2101KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2101BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2101KG-80	0°C to +70°C	20.0 MHz	68-Pin PGA	G-68A
ADSP-2101BG-80	–40°C to +85°C	20.0 MHz	68-Pin PGA	G-68A
ADSP-2101KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2101BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2101KS-80	0°C to +70°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2101BS-80	–40°C to +85°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2101KP-100	0°C to +70°C	25.0 MHz	68-Pin PLCC	P-68A
ADSP-2101BP-100	–40°C to +85°C	25.0 MHz	68-Pin PLCC	P-68A
ADSP-2101KS-100	0°C to +70°C	25.0 MHz	80-Lead PQFP	S-80
ADSP-2101BS-100	–40°C to +85°C	25.0 MHz	80-Lead PQFP	S-80
ADSP-2101KG-100	0°C to +70°C	25.0 MHz	68-Lead PGA	G-68A
ADSP-2101BG-100	–40°C to +85°C	25.0 MHz	68-Lead PGA	G-68A
ADSP-2101TG-50	–55°C to +125°C	12.5 MHz	68-Pin PGA	G-68A
ADSP-2103KP-40 (3.3 V)	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2103BP-40 (3.3 V)	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2103KS-40 (3.3 V)	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2103BS-40 (3.3 V)	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2105KP-55	0°C to +70°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2105BP-55	–40°C to +85°C	13.824 MHz	68-Lead PLCC	P-68A
ADSP-2105KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2105BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115KP-66	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-66	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2115KS-66	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2115BS-66	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2115KST-66	0°C to +70°C	16.67 MHz	80-Lead TQFP	ST-80
ADSP-2115BST-66	–40°C to +85°C	16.67 MHz	80-Lead TQFP	ST-80
ADSP-2115KP-80	0°C to +70°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-80	–40°C to +85°C	20.0 MHz	68-Lead PLCC	P-68A
ADSP-2115KS-80	0°C to +70°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2115BS-80	–40°C to +85°C	20.0 MHz	80-Lead PQFP	S-80
ADSP-2115KST-80	0°C to +70°C	20.0 MHz	80-Lead TQFP	ST-80
ADSP-2115BST-80	–40°C to +85°C	20.0 MHz	80-Lead TQFP	ST-80
ADSP-2115KP-100	0°C to +70°C	25.0 MHz	68-Lead PLCC	P-68A
ADSP-2115BP-100	–40°C to +85°C	25.0 MHz	68-Lead PLCC	P-68A

NOTES
[1]K = Commercial Temperature Range (0°C to +70°C).
B = Industrial Temperature Range (–40°C to +85°C).
T = Extended Temperature Range (–55°C to +125°C).
G = Ceramic PGA (Pin Grid Array).
P = PLCC (Plastic Leaded Chip Carrier).
S = PQFP (Plastic Quad Flatpack).
ST = TQFP (Thin Quad Flatpack)

ORDERING GUIDE

Part Number[1]	Ambient Temperature Range	Instruction Rate (MHz)	Package Description	Package Option
ADSP-2111KG-52	0°C to +70°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2111BG-52	–40°C to +85°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2111KS-52	0°C to +70°C	13.0 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-52	–40°C to +85°C	13.0 MHz	100-Lead PQFP	S-100A
ADSP-2111KG-66	0°C to +70°C	16.67 MHz	100-Pin PGA	G-100A
ADSP-2111BG-66	–40°C to +85°C	16.67 MHz	100-Pin PGA	G-100A
ADSP-2111KS-66	0°C to +70°C	16.67 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-66	–40°C to +85°C	16.67 MHz	100-Lead PQFP	S-100A
ADSP-2111KG-80	0°C to +70°C	20.0 MHz	100-Pin PGA	G-100A
ADSP-2111BG-80	–40°C to +85°C	20.0 MHz	100-Pin PGA	G-100A
ADSP-2111KS-80	0°C to +70°C	20.0 MHz	100-Lead PQFP	S-100A
ADSP-2111BS-80	–40°C to +85°C	20.0 MHz	100-Lead PQFP	S-100A
ADSP-2111TG-52	–55°C to +125°C	13.0 MHz	100-Pin PGA	G-100A
ADSP-2161KP-66[2]	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2161BP-66[2]	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2161KS-66[2]	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2161BS-66[2]	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2162KP-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2162BP-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2162KS-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2162BS-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2163KP-66[2]	0°C to +70°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2163BP-66[2]	–40°C to +85°C	16.67 MHz	68-Lead PLCC	P-68A
ADSP-2163KS-66[2]	0°C to +70°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2163BS-66[2]	–40°C to +85°C	16.67 MHz	80-Lead PQFP	S-80
ADSP-2163KP-100[2]	0°C to +70°C	25 MHz	68-Lead PLCC	P-68A
ADSP-2163BP-100[2]	–40°C to +85°C	25 MHz	68-Lead PLCC	P-68A
ADSP-2163KS-100[2]	0°C to +70°C	25 MHz	80-Lead PQFP	S-80
ADSP-2163BS-100[2]	–40°C to +85°C	25 MHz	80-Lead PQFP	S-80
ADSP-2164KP-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2164BP-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	68-Lead PLCC	P-68A
ADSP-2164KS-40 (3.3 V)[2]	0°C to +70°C	10.24 MHz	80-Lead PQFP	S-80
ADSP-2164BS-40 (3.3 V)[2]	–40°C to +85°C	10.24 MHz	80-Lead PQFP	S-80

NOTES
[1]K = Commercial Temperature Range (0°C to +70°C).
B = Industrial Temperature Range (–40°C to +85°C).
T = Extended Temperature Range (–55°C to +125°C).
G = Ceramic PGA (Pin Grid Array).
P = PLCC (Plastic Leaded Chip Carrier).
S = PQFP (Plastic Quad Flatpack).
[2]Minimum order quantities required. Contact factory for further information.

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